

New Logarithmic Two-Step Flash A/D Converter with Digital Error Correction for MOS Technology

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ABSTRACT

A new technique for realising CMOS logarithmic analog-to-digital (A/D) converters employing a two-step flash architecture suitable for high-frequency operation is described. While the logarithmic operation is achieved by replacing the linear operations of subtraction and multiplication by simple scaling operations, the use of digital error correction and calibration techniques allows to achieve high resolution and high dynamic range logarithmic conversions performance. An example is given to illustrate the proposed technique.

I - Introduction

Logarithmic A/D converters are widely used in communications, instrumentation and hearing aids, among other application areas, where it is needed to adapt the dynamics of signals to the dynamics of the channels used for transmission [1]. Originally, logarithmic converters have been implemented in bipolar technology to explore the inherent exponential I-V characteristic of the transistors [2]. Alternative architectures for implementation in the more cost-effective CMOS technology have also been proposed based on the piecewise approximation of a logarithmic function [3,4]. Examples of these include, among others, the successive approximation [5] and the pulse width modulation type of logarithmic A/D converters [6]. Recently a new type of logarithmic pipeline A/D converter suitable for high-frequency applications has been proposed [7], whereby the signal operations are carried out in the logarithmic domain by simple scaling operations. This paper explores further such technique and proposes a new logarithmic A/D converter employing a two-step flash architecture suitable for implementation in CMOS technology. Digital error correction and calibration techniques traditionally used in linear converters are extended to the logarithmic case. An example is given to illustrate the proposed technique.

II - Two-Step Flash Logarithmic ADC

The conceptual block diagram of the well-known two-step flash A/D converter is shown in Fig. 1 [8]. During the quantization decision cycle, the first flash converter quantizes a sample-and-held input into N digital bits. During the subsequent fine quantization cycle, a reconstructed voltage

corresponding to the coarse N bits is subtracted from the sample-and-held input to generate a residue voltage. This residue voltage is amplified by 2^N and then applied to the second flash converter to extract the least significant bits.

For the realisation of a logarithmic two-step flash A/D converter the operations above have to be carried out in the logarithm domain, where the subtraction is equivalent to a division, and the multiplication by 2^N is equivalent to being raised by 2^N . Such an operation can be explained by representing the input voltage V_{in} as an exponential function of the output digital word D , and which can be written as

$$V_{in} = K \cdot e^{D \cdot \frac{\ln(1/K+1)}{2^N}} \quad (1)$$

where N is the conversion resolution and K is a normalising constant to achieve a full scale input voltage range of 1 V. For $N = 7$ and $K = 0.038$ we obtain the conversion characteristic of Fig. 2 where the output digital code 64 corresponds to an input voltage (V_{ref}) that is the center of the input voltage range in the logarithmic scale. From (1), this gives

$$V_{ref} = K \cdot e^{64 \cdot \frac{\ln(1/K+1)}{128}} = 0.198605 \quad (2)$$

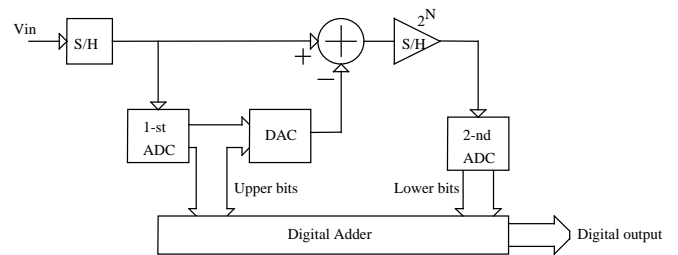


Fig. 1 Conceptual block diagram of a classical, linear two-step flash ADC.

The flash converters must have a logarithmic quantization law to extract both the most and the least significant bits. The first ADC extracts the most significant bits (in a logarithmic scale) which controls the DAC. Then, in the linear case the output of the DAC is subtracted from the input whereas in the logarithmic domain, where the subtraction is equivalent to a division, this operation corresponds to an attenuation that depends on the input digital word of the DAC.

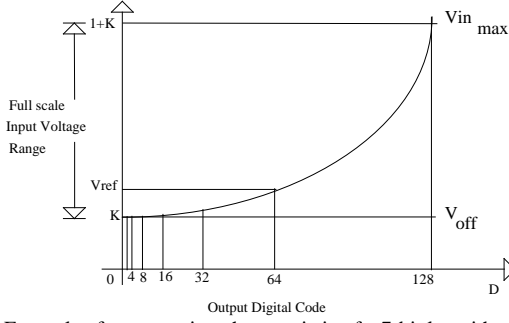


Fig. 2. Example of a conversion characteristic of a 7-bit logarithmic ADC.

Based on this approach the DAC should be replaced by a digitally-controlled logarithmic attenuator whose attenuation factors are given by

$$a_n = e^{-\frac{\ln(1/K+1)}{2^N} \cdot 2^{N2} \cdot n} \quad \text{for} \quad n = 0, \dots, 2^{N1} - 1 \quad (3)$$

with $N1$ and $N2$, respectively, being the resolution bits of the first and second flash converters. Furthermore, to use the same flash converter in both the coarse and fine quantization cycles the residue voltage signal is raised to 2^{N1} .

In order to implement the logarithmic operations described above, we employ the logarithmic two-step flash architecture of Fig. 3, where the raised operation ensures that only one logarithmic scale quantization is needed in both conversion steps.

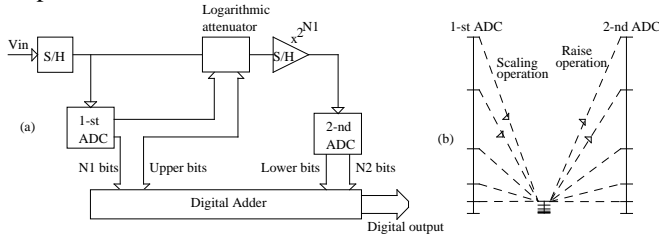


Fig. 3 (a) Block diagram of a logarithmic two-step flash ADC and (b) signal operation at each step of conversion.

III - Improved Two-Step Flash Architecture

A. Basic Architecture

In the basic architecture of Fig. 3, the realisation of the raise function is difficult to implement in integrated circuit form. This, however, is only required to use the same logarithmic scale resolution in both flashes. By abandoning such requirement, and therefore employing a different second flash with the same resolution as for the overall converter, the raised operation is no longer needed and the resulting architecture is similar to a subranging A/D converter [9]. In this case the first and the second ADC's have the threshold voltages respectively given by

$$VT1_n = K \cdot e^{-\frac{\ln(1/K+1)}{2^N} \cdot 2^{N2} \cdot n} \quad \text{for} \quad n = 0, \dots, 2^{N1} - 1 \quad (4)$$

$$VT2_n = K \cdot e^{-\frac{\ln(1/K+1)}{2^N} \cdot n} \quad \text{for} \quad n = 0, \dots, 2^{N2} - 1 \quad (5)$$

However the second ADC must have a resolution of the least significant bit given by

$$LSB = K \cdot e^{-\frac{\ln(1/K+1)}{2^N}} \quad (6)$$

Since in a logarithmic scale the threshold voltages depend on their position in the scale, the difference between two adjacent threshold voltages increase as we increase their position. Consequently, a comparator working in a lower position on the scale has to distinguish a voltage lower than its counterpart in a higher position. The lower comparator needs a higher gain and for the same speed will have a higher power consumption than its counterpart. This problem can be minimized if we introduce an offset in the scale of the second ADC to allow operation in higher positions of the scale. In the logarithmic domain, where the addition is equivalent to a multiplication, this operation corresponds to an amplification dependent on the scale offset introduced. The higher the offset the lower the comparator gain needed. If we shift the second ADC scale near the top of the input range and leave some additional transition steps at the top and at the bottom, it is possible to introduce digital correction of the most significant bits [10]. The precision of the DAC logarithmic attenuator/amplifier can be also calibrated with well known analog and/or digital techniques [10].

Fig. 4 shows the improved architecture with the signal operation at each conversion step and the error correction technique with the amplification step merged in the logarithmic attenuator.

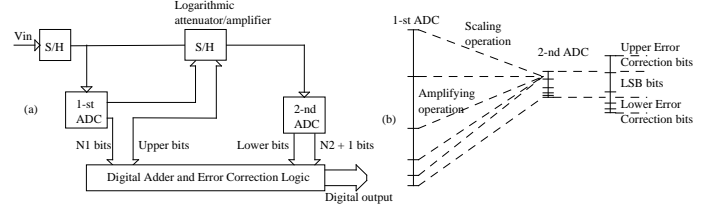


Fig. 4 (a) Improved architecture of the logarithmic two-step flash ADC and (b) signal operation at each step of conversion.

The resulting computer simulated conversion characteristic of the architecture of Fig. 4, for 7-bits resolution with $N1 = 4$ and $N2 = 3 + 1$, is shown in Fig. 5. The extra bit in the second ADC is for digital error correction purposes. The amplification that has been introduced will shift all the threshold voltages of the first ADC to the top of the scale and is given by

$$A_n = e^{-\frac{\ln(1/K+1)}{2^N} \cdot (2^N - 2^{N2} \cdot (1+n))} \quad \text{for} \quad n = 1, \dots, 2^{N1} \quad (7)$$

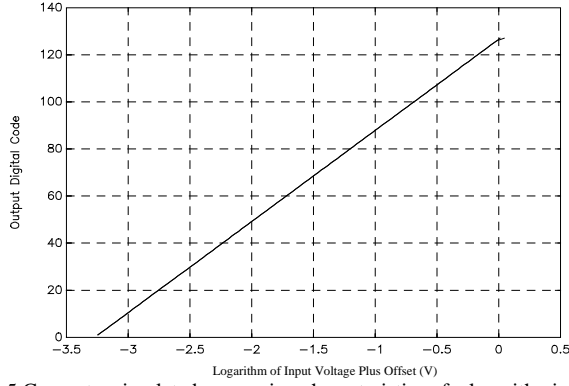


Fig. 5 Computer simulated conversion characteristics of a logarithmic two-step flash ADC based on the architecture of Fig. 4, with 60 dB dynamic range.

Table 1 shows the threshold voltages of the first and second ADC and the attenuation/amplification factors for the case of $N_1 = 4$ and $N_2 = 3$ bits and $K = 0.038$ (60 dB dynamic range), corresponding to a total converter resolution of 7 bits.

Table 1: Attenuation factors of the digitally-controlled logarithmic attenuator with $K = 0.038$.

Comp. stage	Threshold Voltage of the first ADC (V)	Threshold Voltage of the second ADC (V)	Attenuation/amplification factor	Comment	
1	0.0467	0.6353	18.0660	Lower Correction bit	
2	0.0575	0.6519	14.6922		
3	0.0706	0.6690	11.9484		
4	0.0869	0.6865	9.7171		
5	0.1068	0.7045	7.9024	Lower Correction bit LSB bits	
6	0.1314	0.7229	6.4266		
7	0.1615	0.7418	5.2265	LSB bits	
8	0.1986	0.7613	4.2504		
9	0.2442	0.7812	3.4566		
10	0.3003	0.8016	2.8111		
11	0.3692	0.8226	2.2861		
12	0.4540	0.8442	1.8592		
13	0.5583	0.8663	1.5120		Upper Correction bit
14	0.6865	0.8889	1.2296		
15	0.8442	0.9122	1.0000		
16	1.0380	0.9361	0.8133	Upper Correction bit	

B. Linearity Characteristics

Linear A/D converters are usually characterised in terms of *integral nonlinearity* (INL) and *differential nonlinearity* (DNL) characteristics. Similarly, it is also possible to define in the logarithmic domain the INL and DNL characteristics according to [7]

$$INL_{dB} = 20 \cdot (\text{Log}_{10}(VT_{ideal}) - \text{Log}_{10}(VT_{measured})) \quad (8)$$

for the integral nonlinearity, and

$$DNL_{dB} = INL_{dB}(i+1) - INL_{dB}(i) \quad (9)$$

for the differential nonlinearity. For V_{in} varying from K to $(1 + K)$, and assuming a precision of 5% and 0.1% for the resistor string values and attenuation/amplification coefficients, and 60 dB gain comparators, Fig. 6 shows the conversion characteristics and absolute error of the converter of Fig. 4 with 7-bit resolution. Fig. 7 shows the INL and DNL

characteristics of the same converter, with and without digital error correction.

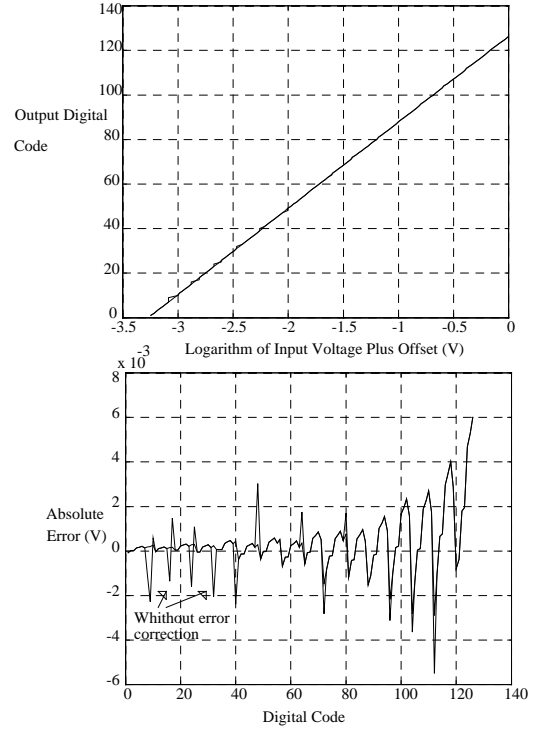


Fig. 6. Conversion characteristics and absolute error of the logarithmic ADC of Fig. 4 for 7 bits resolution, 5% precision on the resistor string, 60 dB gain comparators and 60 dB dynamic range.

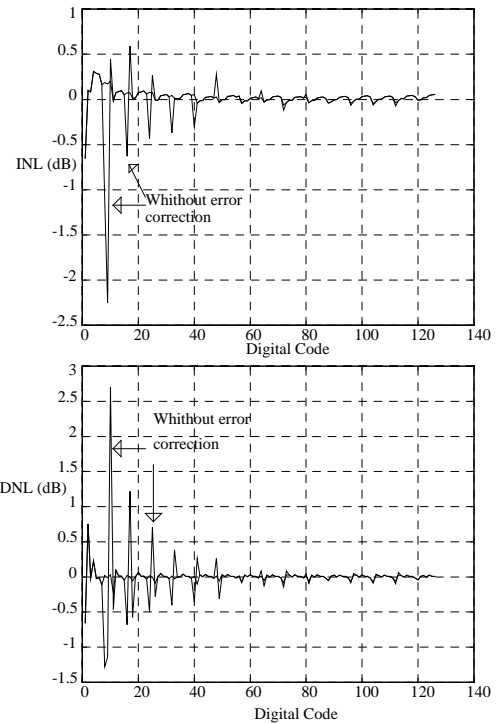


Fig. 7. INL and DNL of the logarithmic ADC of Fig. 4 for 7 bits resolution, 5% precision on the resistor string, 60 dB gain comparators and 60 dB dynamic range.

IV - Design Considerations

By defining the dynamic range (DR), as the ratio between the maximum input voltage range and the LSB given by (6) we obtain [7]

$$DR_{dB} = 20 \cdot \text{Log}_{10} \frac{1}{K \cdot (1 - e^{-\frac{\ln(1/K+1)}{2^N}})} \quad (10)$$

The dynamic range can be designed independently of the converter resolution by defining an appropriated K constant. For the case of 7-bits resolution and 60 dB dynamic range $K = 0.038$.

The threshold voltages of the first and second ADC are obtained by a resistor string. The value of each one is given by [11,12]

$$R_n = R[VT(n) - VT(n-1)] \quad \text{with} \quad R = \sum_{n=1}^N R_n \quad \text{and} \quad n = 1, \dots, N \quad (11)$$

$$R_N = R \cdot VT(N) \quad (12)$$

In such converter the input voltage range is between K and $1 + K$ (1 V full scale). Should the input voltage be referred to ground, then it is necessary to introduce the offset K at the input as shown in Fig. 8.

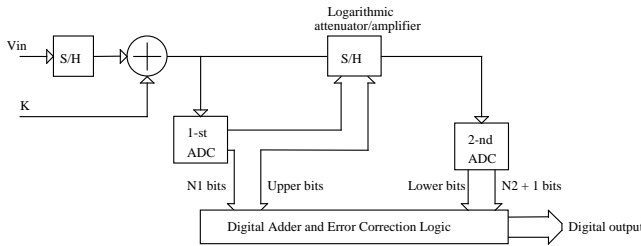


Fig. 8 Block diagram of the logarithmic two-step flash ADC, with the input voltage referred to ground.

V - Conclusions

A new logarithmic analogue-to-digital converter employing a two-step flash architecture suitable for high-frequency operation is MOS technology was described. The logarithmic operation is achieved by replacing the linear operations of subtraction and multiplication by simple scaling operations. This technique allows the use of common digital error correction and calibration techniques targets high resolution and high dynamic range logarithmic A/D converters. An example were given to illustrate the proposed technique.

Acknowledgements

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REFERENCES

- [1] Y. P. Tsvividis and all, "Comanding in Signal Processing", *Electronic Letters* Vol. 26, no.17, pp. 1331-1332, 16th August 1990.
- [2] Henry O. Kunz, "Exponential D/A Converter with a Dynamic Range of Eighth Decades", *IEEE Trans. on Circuits and Systems*, Vol. CAS-25, no. 7, pp. 522-526, July 1978.
- [3] Jorge Guilherme and José E. Franca, "Digitally-Controlled Analogue Signal Processing and Conversion Techniques Employing a Logarithmic Building Block", *Proc. IEEE Int. Symp. on Circuits and Systems*, Vol. 5, pp. 377-380, London, May 1994.
- [4] Jorge Guilherme and José E. Franca, "A Logarithmic Digital-Analog Converter for Digital CMOS Technology", *Proc. IEEE Asia-Pacific Conference on Circuits and Systems*, pp. 490-493, Taiwan, Dec. 1994.
- [5] Gottschalk, "Logarithmic analog-digital converter using switched attenuators", *Rev. Sci. Instrum.*, no. 49, pp. 200-204, Feb. 1978.
- [6] J. N. Lygouras, "Nonlinear ADC with Digitally Selectable Quantizing Characteristic", *IEEE Trans. on Nuclear Science*, Vol. 35, no. 5, pp. 1088-1091, October 1988.
- [7] Jorge Guilherme and José E. Franca, "New CMOS Logarithmic A/D Converters Employing Pipeline and Algorithmic Architectures", *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 529-532, Seattle, May 1995.
- [8] Rudy Van de Plassche, *"Integrated Analog-to-Digital and Digital-to-Analog Converters"*, Kluwer Academic Publishers, 1994.
- [9] Andrew G. F. Dingwall and Victor Zazzu, "An 8-MHz CMOS Subranging 8-Bit A/D Converter", *IEEE Journal of Solid-State Circuits*, vol. SC-20, no. 6, pp. 1138-1143, December 1985.
- [10] Seung-Hoon Lee and Bang-Sup Song, "Digital-Domain Calibration of Multistep Analog-to-Digital Converters", *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1679-1688, December 1992.
- [11] Barry B. Woo, "Digitally Programmable Gain Amplifiers with Arbitrary Range of Integer Values", *Proceedings of the IEEE*, Vol. 68, no. 7, July 1980.
- [12] R. Genin, "Comments on "Digitally Programmable Gain Amplifiers with Arbitrary Range of Integer Values"", *Proceedings of the IEEE*, Vol. 69, no. 5, July 1981.