A LOGARITHMIC DIGITAL-ANALOG CONVERTER FOR DIGITAL CMOS TECHNOLOGY

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ABSTRACT

This paper describes the design and integrated circuit implementation of a logarithmic digital-to-analogue converter employing a digitally-controlled current attenuator whose accuracy depends solely on the matching of transistors. An 8-bit resolution, 80 dB dynamic range prototype chip fabricated in a 1.2 µm digital CMOS technology occupies 1.5 mm^2 and at 5 V supply and 1 MHz conversion rate dissipates 6 mW.

1 - INTRODUCTION

In many applications, ranging from telecommunications to instrumentation and earing aids, there is the need to convert signals using logarithmic techniques to match the dynamic range of the signal to the transmission channel [1]. Several methods for designing D/A converters with a logarithmic input/output relationship are known, namely the piecewise linear approximation using switched attenuators [2], and the use of the exponential law between the base-emitter voltage and the collector current of bipolar transistors [3], among others. For the realization of the former, several implementations proposed in the past have used resistors or capacitors for the linear and accurate division of currents (or voltages) while transistors are employed solely as switches or amplifying elements [4].

In recent years, the rapid development of miniaturised, portable equipments has stimulated much interest in implementing those functions in CMOS technology, basically for power, area and cost efficiency. We investigate in this paper alternative implementations of logarithmic D/A converters using MOS transistors for both the division and the switching functions [5], thus eliminating the need for resistors and capacitors and allowing integration in fully digital CMOS processes.

The proposed piecewise linear approximation converter is based on a logarithmic attenuator that employs the type of current division technique earlier proposed by Bult and Cover [6], which is inherently linear and whose accuracy depends solely on the matching of two MOS transistors. After describing the architecture of the proposed logarithmic DAC, we show how the constituting transistor-only attenuator cells are designed to ensure impedance matching throughout the attenuator chain irrespective of the digitally-selected attenuation factor. An 8-bit resolution, 80 dB dynamic range DAC has been integrated and fabricated in a 1.2 µm CMOS digital technology. The prototype chip occupies 1.5 mm^2 and at 5 V supply and 1 MHz conversion rate dissipates 6 mW.

2 - DIGITALLY-CONTROLLED LOGARITHMIC ATTENUATOR

The core of the logarithmic DAC is formed by a digitally-controlled attenuator dividing the input range in a linear logarithmic scale. This comprises 8 MOS transistor-only cells (Fig. 1), each of which is designed to provide a specific attenuation factor ρ and which when turned *ON* and connected to a terminating resistance *R* should also present a resistance *R* at the input. The latter condition ensures that no other attenuator "knows" whether a given cell is either *ON* or *OFF* and thus rendering the attenuation factors independent.

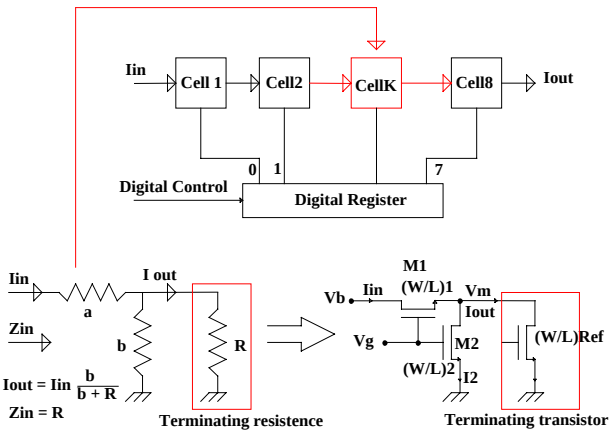

Fig. 1. Basic logarithmic attenuator and one resistive cell.

Referring to Fig. 1, both design conditions can be met if

$$a = (1-\rho)R\ ; \quad b = \frac{\rho}{1-\rho}R\ ; \qquad \rho = \frac{Vout}{Vin} \tag{1}$$

where the attenuator characteristic resistance *R* is a trade-off between speed and matching accuracy. For any digitally-controlled configuration of the attenuator cells the resulting overall attenuation factor on a logarithmic scale is

$$\log D = \log C \cdot \sum_{n=0}^{N-1} a_n 2^n \qquad (2)$$

where a_n are the controlling bits, and C is a constant that corresponds to the minimum step of attenuation and depends on the required dynamic range. For 8-bit resolution and 80 dB dynamic range this gives

$$20 \cdot \log_{10} C = -\frac{80}{256} = -\ 0.3125 \text{ dB} \quad ==> \quad C = 0.96466162 \qquad (3)$$

As indicated in Table 1, the attenuation factor ρ of each one of the 8 basic cells is given by C rised to the power of the binary weight of the corresponding bit. The resulting coeficients a and b are given normalised to the reference resistor (R = 1).

Table 1: Attenuation factors and coefficients of the attenuator.

Cell	Atten. factor ρ	a	b	Weight
8	0.01	0.99	0.010101	128
7	0.1	0.9	0.111111	64
6	0.316227	0.683772	0.462475	32
5	0.562341	0.437658	1.284885	16
4	0.749894	0.250105	2.998308	8
3	0.865964	0.134035	6.460700	4
2	0.930572	0.069427	13.40341	2
1	0.964661	0.035338	27.29784	1

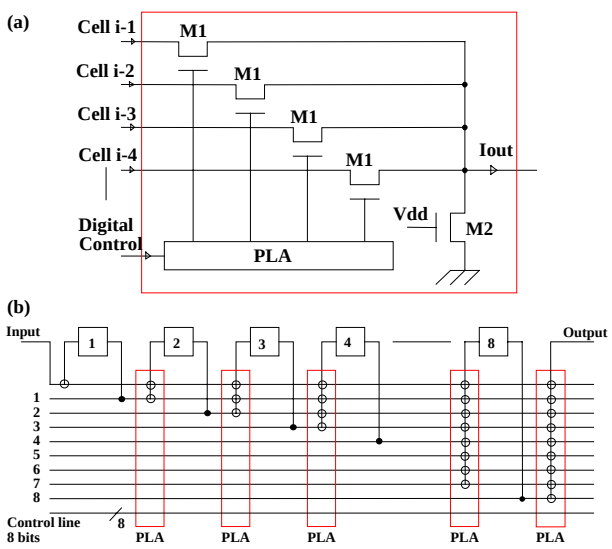

Fig. 2. (a) Analogue and (b) digital control networks of the attenuator.

The analogue and digital control networks of the attenuator are shown in Fig. 2. When one cell is *OFF* within the chain it is necessary to provide a bypass connection to the following cells. This can not be done by using a simple switch connecting the input transistor of the next cell to the output of the preceding one, because the resulting extra input resistance would change the balance between cells. For each cell it is necessary to use instead an analogue multiplexer that incorporates the input transistor of that cell. The number of inputs of the multiplexer is the number of preceding cells. The digital control of the multiplexer selects the entry that corresponds to the closest and previous active cell. This is realised using a PLA network, as also shown in Fig. 2. Since the overall attenuation is the product of the attenuation factors of all 8 cells, independently of their location in the attenuator chain, the first cells must have the largest transistor area because the associated multiplexer has fewer inputs and thus leading to a reduction in the overall silicon area.

The attenuator has been designed with 80 dB dynamic range and an input reference current of 600 μA, leading to a reference transistor of (W/L) = 100/6. The transistor cells M1 and M2 are based on the reference transistor, and knowing that the resistance of an MOS transistor working in the triode region is proportional to L/W. Keeping the channel length equal in both transistors (L = 6 μm), the respective widths are given by

$$W_{M1} = \frac{W_{ref} - 2 \cdot WD}{a} + 2 \cdot WD, \qquad (4)$$

for transistor M1, and

$$W_{M2} = \frac{W_{ref} - 2 \cdot WD}{b} + 2 \cdot WD, \qquad (5)$$

for transistor M2. In the equation above, *WD* is a Spice process parameter. Table 2 gives the resulting equivalent transistor dimensions for the attenuator cells.

Table 2: Sizing of transistors M1 and M2 (L = 6 μm).

Attenuator cell	W of transistor M1 (μm)	W of transistor M2 (μm)
8	2807.07	4.46
7	1429.19	8.23
6	740.69	16.18
5	397.33	33.9
4	227.41	78.01
3	145.86	215.26
2	111.01	893.34
1	101	9818.46

For integrated circuit implementation, transistors M1 and M2 are actually defined as an array of identical unit transistors connected either in series or in parallel. Since transistor M1 always corresponds to $a < 1$, it is defined as a parallel array of unit transistors, as shown in Fig. 3 (a). Their dimensions are calculated from

$$\left(\frac{L}{W}\right)_{M1} = \frac{Lo}{N \cdot (Wo - 2 \cdot WD) + 2 \cdot WD} \qquad (6)$$

where Lo = 6 μm and Wo = 100 μm

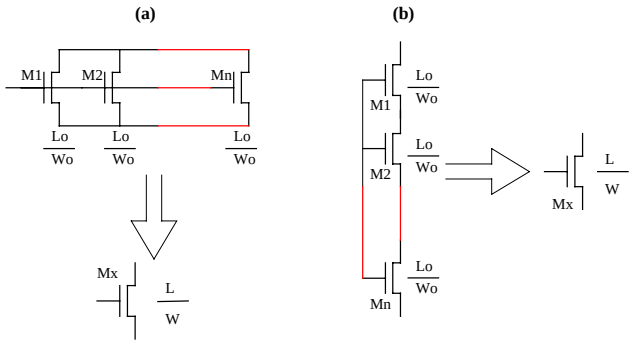

Fig. 3. Equivalences for (a) parallel and (b) serial connections of unit transistors.

For cells 6 to 8 transistor M2 has b < 1 and therefore is also realised as a parallel array of unit transistors. For cells 1 to 5, it results b > 1 and hence transistor M2 is realised as a connection of unit transistors in series, as shown in Fig. 3 (b). Their dimensions are calculated from

$$\left(\frac{L}{W}\right)_{M2} = \frac{Lo}{\frac{Wo - 2 \cdot WD}{N} + 2 \cdot WD} \qquad (7)$$

Since each attenuator factor is the square of the preceding one we can minimise the total number of different transistor cells employed in the attenuator building block by adopting the solution illustrated in Fig. 4, where each cell is realised as the product of two transistor cells equal to the last one. An exception to this is cell 2 which, to minimise area, is better designed as a single cell rather than as twice the very large cell 1. The transistor dimensions used in the complete attenuator are given in Table 3 .

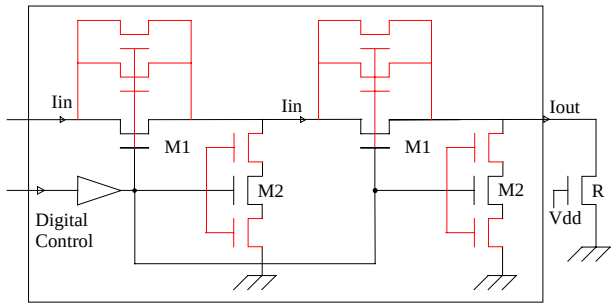

Fig. 4. Connection of two equal cells to form a new one.

Table 3: Final dimensions of transistors (L = 6 µm).

Atten. cell	Transistor M1		Transistor M2		Realisa. of M1	Realisa. of M2
	W (µm) of unit Tran.	Nº of tran. used	W (µm) of unit Tran.	Nº of tran. used		
8	27.68	2 x 4	25.00	2 x 36	parallel	parallel
7	27.68	4	25.00	36	parallel	parallel
6	28.44	2 x 8	25.91	2 x 3	parallel	parallel
5	28.44	8	25.91	3	parallel	parallel
4	26.59	2 x 28	30.75	2 x 2	parallel	series
3	26.59	28	30.75	2	parallel	series
2	35.64	40	36.89	5	parallel	series
1	35.02	80	36.24	10	parallel	series

3 - IC IMPLEMENTATION AND RESULTS

For performing the required logarithmic DAC function the attenuator of Fig. 1 additionally employs one input reference current and the appropriate digital controller, as illustrated in the block diagram of Fig. 5. An amplifier for current voltage conversion is also integrated on-chip. The microphotograph of the prototype chip realised in a 1.2 µm digital CMOS technology is shown in Fig. 6. The waveform displayed in Fig. 7 shows the logarithmic characteristic of the converter.

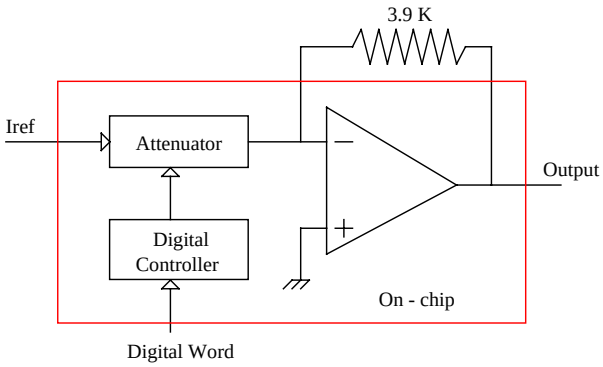

Fig. 5. Block diagram of the logarithmic DAC.

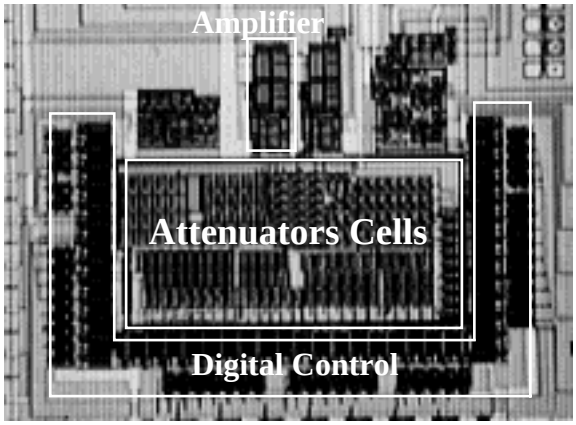

Fig. 6. Chip microphotograph.

Fig. 7. Measured logarithmic characteristic of the DAC.

Fig. 8 compares the measured and nominal conversion characteristics covering 4 decades of the output from 2.34 V to 234 µV. The measured characteristics exhibit some oscillations for the higher attenuation factors, i.e. lower signal levels, due to limitations of the testing environment. Nevertheless, the overall performance of the logarithmic DAC matches well with the target specifications for about 60 dB dynamic range.

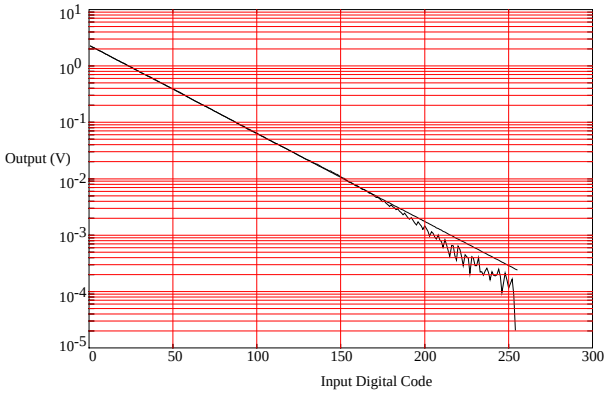

Fig. 8. Measured and simulated characteristic of the logarithmic DAC for 600 µA reference current.

The output relative error of the logarithmic DAC in dB for a reference current of 600 µA is shown in Fig. 9. The precision obtained is better than 2 dB from digital code zero up to digital code 185. A brief summary of the chip characteristics are given in Table 4

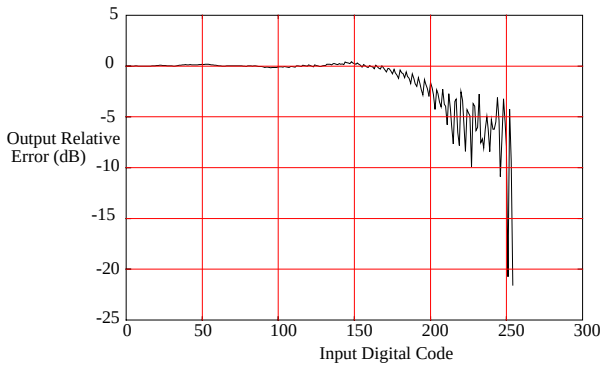

Fig. 9. Measured output relative error of the logarithmic DAC.

Table 4: Summary of measured chip characteristics.

Maximum Output Swing	3 V
Dynamic Range	80 dB
Resolution	8 bits
Maximum Conversion Rate	1 MHz
Power dissipation @ 1 MHz	6 mW
Technology	1.2 µm CMOS (DM/SP)
Voltage supply	5 V
Core Area	1.54 mm^2

4 - CONCLUSIONS

A logarithmic DAC whose accuracy depends solely on the matching of transistors has been described using a digitally-controlled current attenuator that employs only MOS transistors for both the division and the switching functions. Such attenuator together with the associated control logic was integrated in a 1.2 µm digital CMOS technology to realize a full fledged logarithmic DAC with 8-bit resolution and 80 dB dynamic range. At 5 V supply and 1 MHz conversion rate the chip dissipates 6 mW.

5 - ACKNOWLEDGEMENTS

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6 - REFERENCES

[1] Simon Haykin, "*Communication Systems*", John Wiley & Sons, Inc. 1978.

[2] Gottschalk, "Logarithmic analog-digital converter using switched attenuators", *Rev. Sci. Instrum.* Nº49, pp. 200-204, Feb. 1978.

[3] Henry O. Kunz, "Exponential D/A Converter with a Dynamic range of Eight Decades", *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, Nº 7, pp.522-526 July 1978.

[4] Cantarano and G. V. Pallottino, "Logarithmic Analog-to-Digital Converters: A Survey", *IEEE Trans. Instrumentation and Measurement*, Vol. IM-22, Nº3 pp. 201-213, September 1973.

[5] Jorge Guilherme and José E. Franca, "Digitally-Controlled Analogue Signal Processing and Conversion Techniques Employing a Logarithmic Building Block", *Proc. IEEE Int. Symp. on Circuits and Systems*, Vol. 5 pp 377-380. , London May 1994.

[6] Klaas Bult and Govert J. G. M. Geelen,"An Inherent Linear and Compact MOST-Only Current Division Technique", *IEEE Jornal of Solid-State Circuits*, Vol. 27, Nº12 pp. 1730-1735, December 1992.